IN THE SPECIFICATION

Insert new paragraph at page 11 between lines 5 and 6:

The layout view of FIG. 2 also shows that, in both the NMOS output transistor 11 and in the NMOS dummy transistor 10, the P+ contact layer 27 (which is an area of P-well 22, as shown in Fig. 1(b)) substantially surrounds the structures including the gates, sources, and drains of the transistors 10 and 11, forming an almost-closed loop in each transistor. This is also indicated by cross-sectional view Fig. 1(b) of the same embodiment, which shows four areas 27 that lie on either side of the gates 14 and 21, the drains 15 and 25, and the sources 16 and 26.